Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 32 (previously presented): A charge sampling circuit, comprising:

a control signal generator for controlling an analog input signal to the charge sampling circuit; and

an integrator for integrating directly the analog input signal during a sampling phase responsive to a sampling signal from the control signal generator, wherein a current of the analog input signal is integrated to an integrated charge for producing one of a proportional voltage sample and a proportional current sample at a signal output upon completion of the sampling phase.

Claim 33 (previously presented): The charge sampling circuit according to claim 32, further comprising:

a sampling switch having a signal input for analog input signals, a signal output connected to a signal input of said integrator, and a control input connected to a sampling signal output of said control signal generator for controlling the switch to be on only when said sampling signal from the generator is in a sampling phase.

Claim 34 (previously presented): The charge sampling circuit according to claim 32, wherein the control signal generator controls the integrator to hold the sample until a resetting signal from the generator is applied to a control input of the integrator.

Claim 35 (previously presented): The charge sampling circuit according to claim 32, wherein if said sampling phase is from time t_1 to time t_2, said sample represents the instant value of said analog signal at time $t_S = (t_1 + t_2) / 2$ and differs from said instant value with a coefficient comprising a constant part and a frequency

dependent part $(\sin(2\pi f_i \Delta t)) / (2\pi f_i \Delta t)$, where f_i is the frequency of the ith component of said analog signal and $\Delta t = (t_2 - t_1) / 2$.

Claim 36 (previously presented): A differential charge sampling circuit, comprising:

a first charge sampling circuit having a first integrator;

a second charge sampling circuit having a second integrator;

a first analog input being a signal input of the first charge sampling circuit;

a second analog input being a signal input of the second charge sampling circuit;

a first signal output being a signal output of the first charge sampling circuit;

a second signal output being a signal output of said second charge sampling circuit; and

a common control signal generator for controlling an analog input signal provided to the first and second analog inputs, wherein the first and second integrators integrate a respective portion of the analog input signal during a sampling phase responsive to a sampling signal from the common control signal generator.

Claim 37 (previously presented): The differential charge sampling circuit according to claim 36, wherein the first integrator and the second integrator form a single differential integrator having two inputs for integrating a differential current of said analog signal and for producing differential samples at said first signal output and at the second signal output of the differential charge sampling circuit.

Claim 38 (previously presented): A band-pass charge sampling circuit, comprising:

a control signal generator for controlling a first and second portion of a differential analog signal;

a first signal input for receiving the first portion of the differential analog signal;

a second signal input for receiving the second portion of the differential analog signal;

an integrator; and

a weighting-and-sampling element for processing the differential analog signal during a weighting-and-sampling phase responsive to a weighting-and-sampling signal from said control signal generator, wherein a current of said differential analog signal passes through said weighting-and-sampling element only when said weighting-and-sampling signal is in a weighting-and-sampling phase, said control signal generator for controlling an output signal of said weighting-and-sampling element to be integrated by the integrator during said weighting-and-sampling phase, and a current of the output signal of said weighting-and-sampling element is integrated to an integrated charge for producing one of a proportional voltage sample and a proportional current sample at a signal output upon completion of said weighting-and-sampling phase.

Claim 39 (previously presented): The band-pass charge sampling circuit according to claim 38, further comprising:

a first switch having

a signal input coupled to the first signal input of the band-pass charge sampling circuit for receiving the first portion of the differential analog signal,

a signal output connected to a signal input of said weighting-and-sampling element, and

a control input connected to a clock output of said control signal generator for controlling the first switch to be on only when a first clock signal is received; and

a second switch having

a signal input coupled to the second signal input of the band-pass charge sampling circuit for receiving the second portion of the differential analog signal,

a signal output connected to said signal input of said weighting-and-sampling element, and

a control input connected to an inverse clock output of said control signal generator for controlling the switch to be on only when a second clock signal is received, wherein said weighting-and-sampling element includes a control input connected to a weighting-and-sampling signal output of said control signal generator

whereby the current of said analog signal passes through said weighting-and-sampling element only when said weighting-and-sampling signal is in a weighting-and-sampling phase containing a number of cycles, *n*, of the first and second clock signals, the current of said analog signal is controlled by said weighting-and-sampling signal using one of a constant, a linear, and a Gaussian weighting function, and the integrator includes a control input connected to a resetting signal output of said control signal generator.

Claim 40 (previously presented): The band-pass charge sampling circuit according to claim 38, wherein the control signal generator controls the integrator to hold the sample until a resetting phase controlled by said resetting signal begins.

Claim 41 (previously presented): The band-pass charge sampling circuit according to claim 38, wherein said samples represent a base-band content of said analog signal, and the output frequency is $f_{out} = |f_{in} - (2p-1)f_c|$ for $2(p-1)f_c \leq f_{in} \leq 2pf_c$, where f_{in} is one of a plurality of frequency components of said analog signal, f_c is a frequency of said clock, and p is an integer greater than or equal to 1, and a phase of said output frequency depends on a phase of said f_{in} and a phase of said f_c, wherein p=1 defines a major frequency response range and the same shape of frequency response is repeated for p>1 but the amplitudes are reduced, and for a given p, the same output frequency is obtained for frequencies $f_{in1} < (2p-1)f_c$ and $f_{in2} > (2p-1)f_c$ when $(2p-1)f_c - f_{in1} = f_{in2} - (2p-1)f_c$ but with different phases, and the bandwidth and the shape of said frequency response depend on said number of cycles, *n*, the larger *n* the narrower the bandwidth, and said weighting function and said band-pass charge sampling circuit operate simultaneously as a filter, a mixer and a sampler.

Claim 42 (previously presented): A differential band-pass charge sampling circuit, comprising:

a common control signal generator for controlling a first and second portion of a differential analog signal;

a first band-pass charge sampling circuit, having

a first signal input operating as a first signal input of the differential band-pass charge sampling circuit for receiving the first portion of the differential analog signal,

a second signal input operating as a second signal input of the differential band-pass charge sampling circuit for receiving the second portion of the differential analog signal,

a first integrator having an output operating as a first signal output of the differential band-pass charge sampling circuit, and

a first weighting-and-sampling element coupled to the first integrator; and

a second band-pass charge sampling circuit, having

a first signal input coupled to the second input of the first band-pass charge sampling circuit,

a second signal input coupled to the first input of the first band-pass charge sampling circuit,

a second integrator having an output operating as a second signal output of the differential band-pass charge sampling circuit, and

a second weighting-and-sampling element coupled to the second integrator, wherein the first and second weighting-and-sampling elements process the differential analog signal during a weighting-and-sampling phase responsive to a weighting-and-sampling signal from said control signal generator, a current of said differential analog signal passes through said weighting-and-sampling elements only when said weighting-and-sampling signal is in a weighting-and-sampling phase, said control signal generator is adapted for controlling an output signal of each first and second weighting-and-sampling elements to be integrated by the respective first and second integrators during said weighting-and-sampling phase, and a current of each output signal of the first and second weighting-and-sampling elements is integrated to an integrated charge for producing one of a proportional voltage sample and a proportional current sample at the respective first and second signal outputs of the differential band-pass charge sampling circuit upon completion of said weighting-and-sampling phase.

Claim 43 (previously presented): The differential band-pass charge sampling circuit according to claim 42, wherein the first and second integrators form a single differential integrator for integrating the differential current of said analog signal and for producing differential samples at the first signal output and the second signal output of the differential band-pass charge sampling circuit.

Claim 44 (previously presented): A parallel charge sampling circuit, comprising:

a common control signal generator; and

a plurality of charge sampling circuits, each respective charge sampling circuit having

a first analog input being a signal input of the respective charge sampling circuit and responsive to a controlling signal from the common control signal generator; and

an integrator for integrating the analog input signal during a sampling phase responsive to a sampling signal from the common control signal generator;

wherein all analog first signal inputs are connected together as a common analog signal input of said parallel charge sampling circuit, a multiplexer having a plurality of signal inputs connected to the signal outputs of said charge sampling circuits respectively, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output for multiplexing the outputs of said charge sampling circuits to the output of said parallel charge sampling circuit when the outputs of said charge sampling circuits are in holding phases.

Claim 45 (currently amended): A differential parallel charge sampling circuit[,] comprising a number of differential charge sampling circuits, each ~~having a~~ differential charge sampling circuit[,] comprising:

a first charge sampling circuit having a first integrator;

a second charge sampling circuit having a second integrator;

a first analog input being a signal input of the first charge sampling circuit;

a second analog input being a signal input of the second charge sampling circuit;

a first signal output being a signal output of the first charge sampling circuit;

a second signal output being a signal output of said second charge sampling circuit; and

a common control signal generator for controlling an analog input signal provided to the first and second analog inputs[,];

wherein all first inputs are connected together as a common first signal input of said parallel charge sampling circuit for receiving a first end of a differential analog signal, all second inputs are connected together as a common second signal input of said parallel charge sampling circuit for receiving a second end of said differential analog signal, and all control signal generators of said charge sampling circuits are replaced by a common control signal generator, a multiplexer having a plurality of signal input pairs connected to the signal output pairs of said charge sampling circuits respectively, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output pair for multiplexing the output pairs of said charge sampling circuits to the output pair of said parallel charge sampling circuit when the output pairs of said charge sampling circuits are in holding phases.

Claim 46 (previously presented): The parallel charge sampling circuit according to claim 44, wherein said common control signal generator has a clock input, a plurality of sampling signal outputs, a plurality of resetting signal outputs, and a plurality of multiplexing signal outputs for generating said plurality of sampling signals at the sampling signal outputs connected to the control inputs of the switches of said charge sampling circuits respectively, and for generating said plurality of resetting signals at said resetting signal outputs connected to the control inputs of the integrators of the charge sampling circuits respectively, and said plurality of multiplexing signals are generated at the multiplexing signal outputs, and said resetting signals, said sampling signals and said multiplexing signals are evenly timeinterleaved.

Claim 47 (previously presented): A parallel band-pass charge sampling circuit comprising a plurality of band-pass charge sampling circuits each having band-pass charge sampling circuit, comprising:

a control signal generator for controlling a first and second portion of a differential analog signal;

a first signal input for receiving the first portion of the differential analog signal;

a second signal input for receiving the second portion of the differential analog signal;

an integrator; and

a weighting-and-sampling element for processing the differential analog signal during a weighting-and-sampling phase responsive to a weighting-and-sampling signal from said control signal generator, wherein all first signal inputs are connected together as a common signal input of said parallel band-pass charge sampling circuit for receiving a first end of a differential analog signal, all second signal inputs are connected together as a common second signal input of said parallel band-pass charge sampling circuit for receiving a second end of a differential analog signal, the first switches are one of separate and merged, the second switches are one of separate and merged, and all control signal generators in said band-pass charge sampling circuits are replaced by a common control signal generator, and a multiplexer having a plurality of signal inputs connected to the signal outputs of said band-pass charge sampling circuits, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output for multiplexing the outputs of said band-pass charge sampling circuits to the signal output when the signal outputs of said band-pass charge sampling circuits are in holding phases, whereby the signal output is the signal output of said parallel band-pass charge sampling circuit.

Claim 48 (previously presented): A parallel band-pass charge sampling circuit comprising a plurality of band-pass charge sampling each having:

a common control signal generator for controlling a first and second portion of a differential analog signal;

a first band-pass charge sampling circuit, having

a first signal input operating as a first signal input of the differential band-pass charge sampling circuit for receiving the first portion of the differential analog signal,

a second signal input operating as a second signal input of the differential band-pass charge sampling circuit for receiving the second portion of the differential analog signal,

a first integrator having an output operating as a first signal output of the differential band-pass charge sampling circuit, and

a first weighting-and-sampling element coupled to the first integrator; and

a second band-pass charge sampling circuit, having

a first signal input coupled to the second input of the first band-pass charge sampling circuit,

a second signal input coupled to the first input of the first band-pass charge sampling circuit,

a second integrator having an output operating as a second signal output of the differential band-pass charge sampling circuit, and

a second weighting-and-sampling element coupled to the second integrator;

wherein all first signal inputs are connected together as a common first signal input of said parallel band-pass charge sampling circuit for receiving a first end of a differential analog signal, all second signal inputs are connected together as a common second signal input of said parallel band-pass charge sampling circuit for receiving a second end of a differential analog signal, all the first switches in said first band-pass charge sampling circuits are one of separate and merged, all the second switches in said first band-pass charge sampling circuits are one of separate and merged, all the first switches in said second band-pass charge sampling circuits are one of separate and merged, all the second switches in said second band-pass charge sampling circuits are one of separate and merged, all control signal generators of said band-pass charge sampling circuits are replaced by a common control signal generator, and a multiplexer with said number of signal input pairs connected to the signal output pairs of said band-pass charge sampling circuits, control inputs connected to multiplexing signal outputs of said common control signal

generator, and an output pair for multiplexing the output pairs of said band-pass charge sampling circuits to the signal output pair when the signal output pairs of said band-pass charge sampling circuits are in holding phases, whereby the signal output pair is the signal output pair of said parallel band-pass charge sampling circuit.

Claim 49 (previously presented): The parallel band-pass charge sampling circuit of claim 48, wherein the common control signal generator includes a clock input, a clock output, an inverse clock output, a plurality of weighting-and-sampling signal outputs, a plurality of resetting signal outputs and a plurality of multiplexing signal outputs, whereby the clock input is the clock input of said parallel band-pass charge sampling circuit for use in generating a clock signal at the clock output of said common signal control generator connected to the control inputs of all first switches of said band-pass charge sampling circuits, and an inverse clock at the inverse clock output connected to the control inputs of all second switches of said band-pass charge sampling circuits, said plurality of weighting-and-sampling signal outputs are connected to the control inputs of all weighting-and-sampling elements of said band-pass charge sampling circuits, said plurality of resetting signal outputs are connected to the control inputs of all integrators of said band-pass charge sampling circuits, and said plurality of multiplexing signals, resetting signals, sampling signals, and multiplexing signals are evenly timeinterleaved.

Claim 50 (previously presented): The charge sampling circuit according to claim 32, further comprising an analog frequency compensating circuit having a signal input for receiving an analog signal, and a signal output, with a frequency response proportional to $(2\pi f_i \Delta t) / (\sin (2\pi f_i \Delta t))$, wherein the signal output is connected to the signal input of said charge sampling circuit.

Claim 51 (previously presented): The charge sampling circuit according to claim 36, further comprising an analog frequency compensating circuit having a signal input pair for receiving an analog signal, and a signal output pair, with a frequency response proportional to $(2\pi f_i \Delta t) / (\sin (2\pi f_i \Delta t))$, wherein the signal

output pair is connected to the first signal input and the second signal input of said charge sampling circuit.

Claim 52 (previously presented): The charge sampling circuit according to claim 32, further comprising a digital frequency compensating circuit with a frequency response proportional to $(2\pi f_i \Delta t) / (\sin (2\pi f_i \Delta t))$ connected after an A/D converter converting the signal output of said charge sampling circuits to a digital signal.

Claim 53 (previously presented): The charge sampling circuit according to claim 36, further comprising a digital frequency compensating circuit with a frequency response proportional to $(2\pi f_i \Delta t) / (\sin (2\pi f_i \Delta t))$ connected after an A/D converter converting the signal output pair of said charge sampling circuits to a digital signal.

Claim 54-57 (canceled).

Claim 58 (previously presented): A method of charge sampling, comprising the steps of:

integrating directly an analog input signal during a sampling phase, wherein the current of the analog input signal is integrated to an integrated charge; and

producing one of a proportional voltage and a proportional current sample of said integrated charge at the end of said sampling phase.

Claim 59 (currently amended): The method according to claim 58, wherein if said sampling phase is from time [t_i] t_1 to time t_2, said sample represents the instant value of said analog signal at time $t_s = ([t_i] t_1 + t_2) / 2$ and differs from said instant value with a coefficient consisting of a constant part and a frequency dependent part $(\sin (2\pi f_i \Delta t)) / (2\pi f_i \Delta t)$, where f_i is the frequency of the ith component of said analog signal and $\Delta t = (t_2 - t_1) /2$.

Claim 60 (previously presented): The method according to claim 58, wherein said analog input signal is a differential analog signal, and said one of a proportional voltage and a proportional current sample of said integrated charge is a differential signal.

Claim 61 (currently amended): A method of charge sampling, comprising the steps of:

weighting a first and second end of a differential analog signal during a weighting-and-sampling phase;

integrating the weighted signal during said weighting-and-sampling phase, wherein the current of the weighted signal is integrated to an integrated charge; and

producing one of a proportional voltage and a proportional current sample at the end of said weighting-and-sampling phase.

Claim 62 (new): The band-pass charge sampling circuit of claim 38, wherein the band-pass charge sampling circuit is a first of two band-pass charge sampling circuits included in a two-step band-pass charge sampling circuit, the first band-pass charge sampling circuit for producing signal samples at the signal output or output pair of said first band-pass charge sampling circuit with a first sample rate, the two-step band-pass charge sampling circuit comprising:

a chopping circuit for chopping the signal from the first band-pass charge sampling circuit symmetrically in time at its signal output or output pair with the frequency of a clock signal equal to said first sample rate; and

a differential-out amplifier for amplifying the signal from the chopping circuit differentially at its signal output pair;

wherein the first signal input and the second signal input of a second band-pass charge sampling circuit are connected to the signal output pair of said amplifier for producing signal samples at the signal output or output pair with a second sample rate.

Claim 63 (new): The band-pass charge sampling circuit of claim 62, wherein the two-step band-pass charge sampling circuit comprises:

a clock signal generator having a clock input for receiving a first clock signal used by the first band-pass charge sampling circuit, and generating a second clock signal simultaneously fed to a clock input of said chopping circuit and a clock input of said second band-pass charge sampling circuit.

Claim 64 (new): The band-pass charge sampling circuit of claim 38, wherein the band-pass charge sampling circuit is a first of two band-pass charge sampling circuits included in a front-end sampling radio receiver apparatus, the apparatus comprising:

a low pass filter for receiving and filtering a radio signal, the low pass filter having a bandwidth up to twice a clock frequency associated with the band-pass charge sampling circuits;

a low noise amplifier for producing a differentially amplified radio signal from the filtered signal;

a local oscillator for producing an I-clock signal at its signal output; and

a $\pi/2$ phase shifter with a signal input connected to the local oscillator for producing a Q-clock signal at its signal output with the same amplitude and $\pi/2$ phase shift with respect to said I-clock signal;

wherein two ends of the signal output pair of said low noise amplifier are respectively connected both to the first band-pass charge sampling circuit and to a second band-pass charge sampling circuit respectively, said I-clock signal output is connected to the clock input of said first band-pass charge sampling circuit, and said Q-clock signal output is connected to the clock input of said second band-pass charge sampling circuit, for producing base-band I-samples of said radio signal at the signal output or output pair of said first band-pass charge sampling circuit, base-band Q samples of said radio signal at the signal output or output pair of said second band-pass charge sampling circuit.

Claim 65 (new): The band-pass charge sampling circuit of claim 64, wherein:

the local oscillator, the phase shifter and the clock generators of the first and second band-pass charge sampling circuits are combined for producing differential I-clock signals and Q-clock signals;

the base-band I-sample and Q-samples are converted by one of two separate analog-to-digital converters or by a single analog-to-digital converter with multiplexing to digital signals; and

the digital signals are processed by a digital signal processing unit.